DSP56824ADM

User's Manual

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SECTION 1

QUICK START GUIDE

1.1 DSP56824ADM OVERVIEW

The DSP56824 Application Development Module (DSP56824ADM) was designed to operate with the Motorola Application Development System (ADS). Use of the DSP56824ADM with the Motorola ADS facilitates development, debug, and test of complex software applications and hardware products designed for the DSP56824. Detailed information about the Motorola ADS is provided in the Motorola ADS User's Manual (order # DSPADSUM/AD).

Subsection 1.2 of this document gives a summary description of the equipment required to use the module with the Motorola ADS.

Subsection 1.3 describes installation instructions, including the following:

- Preparing the module for installation
- Installing the module
- Installing the software
- Testing the installation

Note: Detailed information about the design and operation of the DSP56824ADM is provided in this manual in **Section 2** and **Appendices A** and **B**.

1.2 REQUIRED USER-SUPPLIED EQUIPMENT

For use with the Motorola ADS (and the appropriate interface card), the user must supply one of the following host computer systems:

- PC-compatible computer (486 class or higher) with the following:
  - MS-DOS version 6.0 or later, Windows 3.1 or later, or Windows 95
  - 8 Mbytes RAM
  - One open 16-bit ISA expansion slot
  - One bank of free I/O addresses in the range of $100–$102, $200–202, or $300–$303
  - CD-ROM drive
  - Hard drive with 4 Mbytes of free disk space
  - Mouse

- Hewlett Packard HP7xx Workstation running HPUX Version 9.x (Version 10.x is not supported), one open EISA expansion slot, CD-ROM drive, and a mouse
- Sun Microsystems Sun 4 Workstation running Sun Operating System Release 4.1.1 or later (or Solaris Release 2.5 or later), one open SBus expansion slot, a CD-ROM drive, and a mouse

1.3 INSTALLATION PROCEDURE

Installation requires four basic steps:

1. Preparing the DSP56824ADM board
2. Installing the module
3. Installing the software
4. Testing the installation

1.3.1 Preparing the DSP56824ADM

CAUTION

Because all electronic components are sensitive to the effects of electrostatic discharge (ESD) damage, correct procedures should be used when handling all components in this kit and inside the supporting personal computer. Use the following procedures to minimize the likelihood of damage due to ESD:

- **Always handle all static-sensitive components only in a protected area, preferably a lab with conductive (anti-static) flooring and bench surfaces.**
- **Always use grounded wrist straps when handling sensitive components.**
- **Never remove components from anti-static packaging until required for installation.**
- **Always transport sensitive components in anti-static packaging.**

Locate the jumper blocks JG1–JG17 on the DSP56824ADM board, as shown in **Figure 1-1**. **Table 1-1** describes the jumper group settings for use with the Motorola ADS. Read the

technical summary in **Section 2** of this manual for additional information about the DSP56824ADM board and its components.

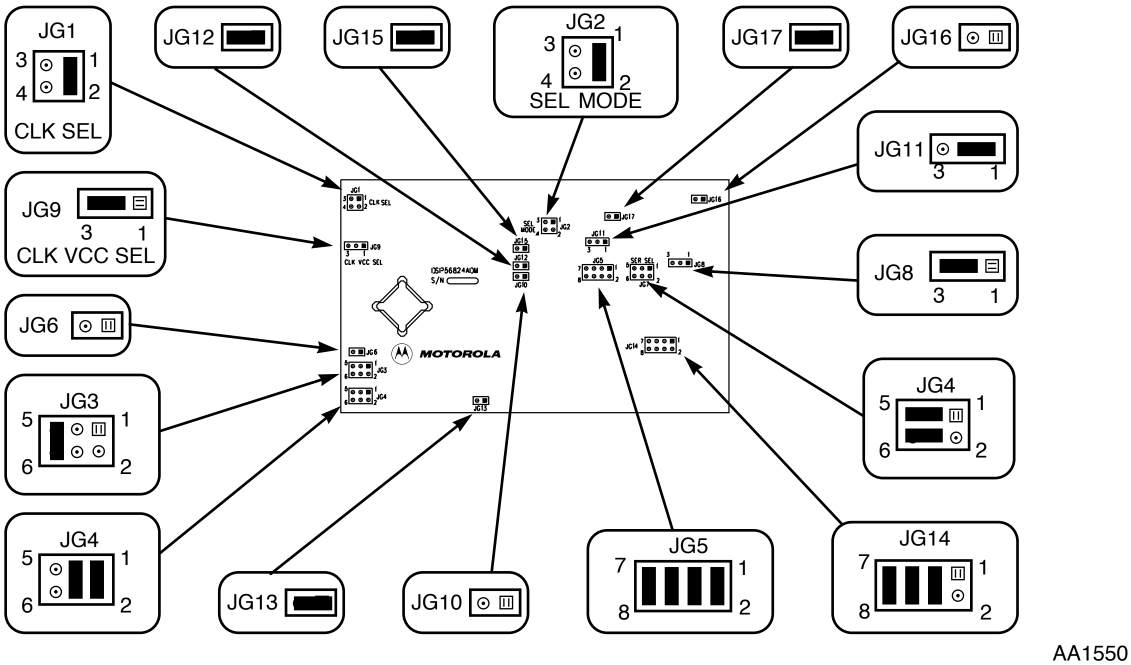


Figure 1-1 DSP56824ADM Quick Jumper Reference

Table 1-1 DSP56824ADM Default Jumper Options

Jumper Group	Comment	Jumpers Connections
JG1	Selects oscillator (U14) for clock input	1–2
JG2	Selects Mode 2 operation upon exit from reset	1–2
JG3	Selects Program memory with external Non-Volatile Static RAM (NVSRAM)	5–6
JG4	Selects Data memory	1–2, 3–4
JG5	Selects on-board codec	1–2, 3–4, 5–6, 7–8
JG6	Reserved	NC
JG7	Selects serial port connection to DSP	3–5, 4–6
JG8	Selects codec High Bandpass mode	2–3

Table 1-1 DSP56824ADM Default Jumper Options (Continued)

JG9	Selects 8-pin oscillator V_{CC} = +5 V	2–3
JG10	Selects high input frequencies	NC
JG11	Selects codec output to 1.7 V peak @ 300 Ω	1–2
JG12	Selects PB14 Light-Emitting Diode (LED)	1–2
JG13	Selects external NVSRAM 32K × 16	1–2
JG14	Power in to 3.3 V and 5 V regulators	3–4, 5–6, 7–8
JG15	Enable on-board reset logic	1–2
JG16	Codec input mono	NC
JG17	Codec output mono on both channels (left and right)	1–2

1.3.2 Installing the Module

Figure 1-2 shows the interconnection diagram for connecting the PC to the DSP56824ADM board. Using the instructions in the ADS User's Manual, connect the Command Converter to the DSP56824ADM board. Power for the DSP56824ADM is supplied from an external 9–12 VDC power supply.

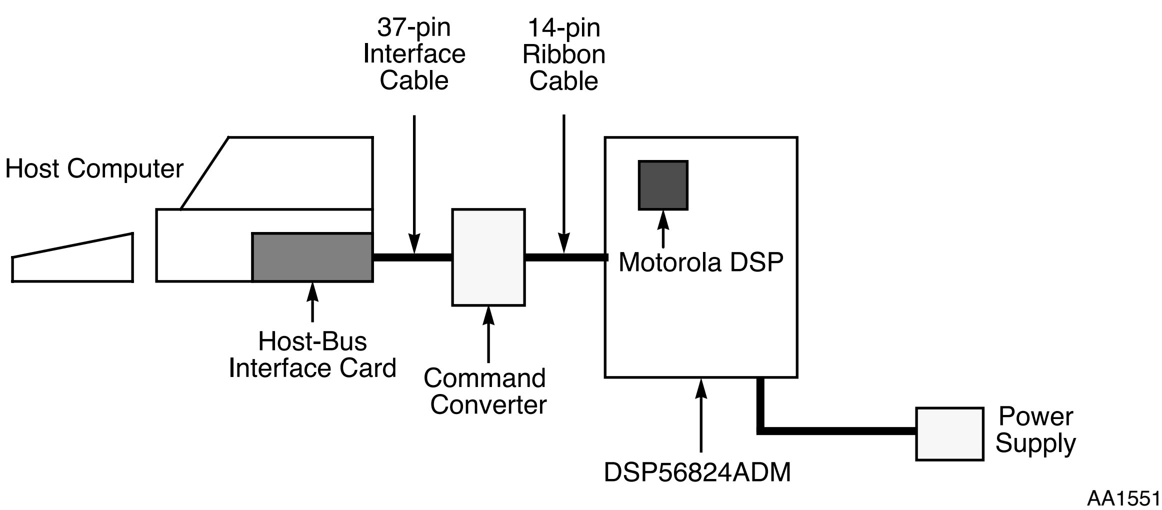


Figure 1-2 Application Development

1.3.3 Installing the Software

Refer to the Motorola Application Development System User's Manual for detailed instructions about installation and use of the ADS software.

1.3.4 Testing the DSP56824ADM Installation

Refer to the Motorola Application Development System User's Manual for detailed information regarding evaluation and testing of an installed ADS system.

SECTION 2

DSP56824ADM TECHNICAL SUMMARY

2.1 DSP56824ADM DESCRIPTION AND FEATURES

The DSP56824ADM is designed as a versatile Digital Signal Processor (DSP) development card that can be used with the Motorola Applications Development System (ADS) and can also be plugged into other cards to permit special user configurations. Two 70-pin connectors, J1 and J2, located on the bottom of the Printed Circuit Board (PCB), allow access to all the DSP signals, including V_{DD} (3.3 V) and V_{SS} (GND). An overview description of the DSP56824ADM is also provided in the DSP56824ADM Product Information (DSP56824ADMP/D) included with this kit. The main features of the DSP56824ADM include the following:

- DSP56824 16-bit DSP
- External Fast Static RAM (FSRAM) memory
  - 64K × 16 program memory
  - 64K × 16 data memory
- 32K × 16 External Non-Volatile Static RAM (NVSRAM) memory
- 13-bit linear codec with voice input and output jacks
- Socketed on-board 20 MHz oscillator for DSP system clock
- Manual DSP reset button S1
- Manual interrupt button S2 for $\overline{\text{IRQA}}$
- Light Emitting Diode (LED) power indicator (LED1)
- LED for user debug operations (LED2)
- Two on-board 70-pin expansion connectors
- Joint Test Action Group (JTAG) port connector for Motorola's ADS that provides an enhanced development environment including a high-speed data transfer port to a host PC ISA bus

2.2 DSP56824 DESCRIPTION

A full description of the DSP56824, including functionality and user information, is provided in the following documents included as a part of this kit (either as printed copies or on the documentation CD-ROM):

- DSP56824 Technical Data (DSP56824/D): Provides features list and specifications including signal descriptions, dc power requirements, ac timing requirements, and available packaging
- DSP56824 User's Manual (DSP56824UM/AD): Provides an overview description of the DSP and detailed information about the on-chip components including the memory and I/O maps, peripheral functionality, and control and status register descriptions for each subsystem
- DSP56800 Family Manual (DSP56800FM/AD): Provides a detailed description of the core processor including internal status and control registers and a detailed description of the family instruction set

Refer to these documents for detailed information about chip functionality and operation.

2.3 MEMORY

The DSP56824ADM uses the following memory external to the DSP56824:

- 64K × 16-bit FSRAM for external program memory
- 64K × 16-bit FSRAM for external data memory
- 32K × 16-bit NVSRAM program memory

Figure 2-1 shows a functional block diagram of the DSP56824ADM including the memory devices.

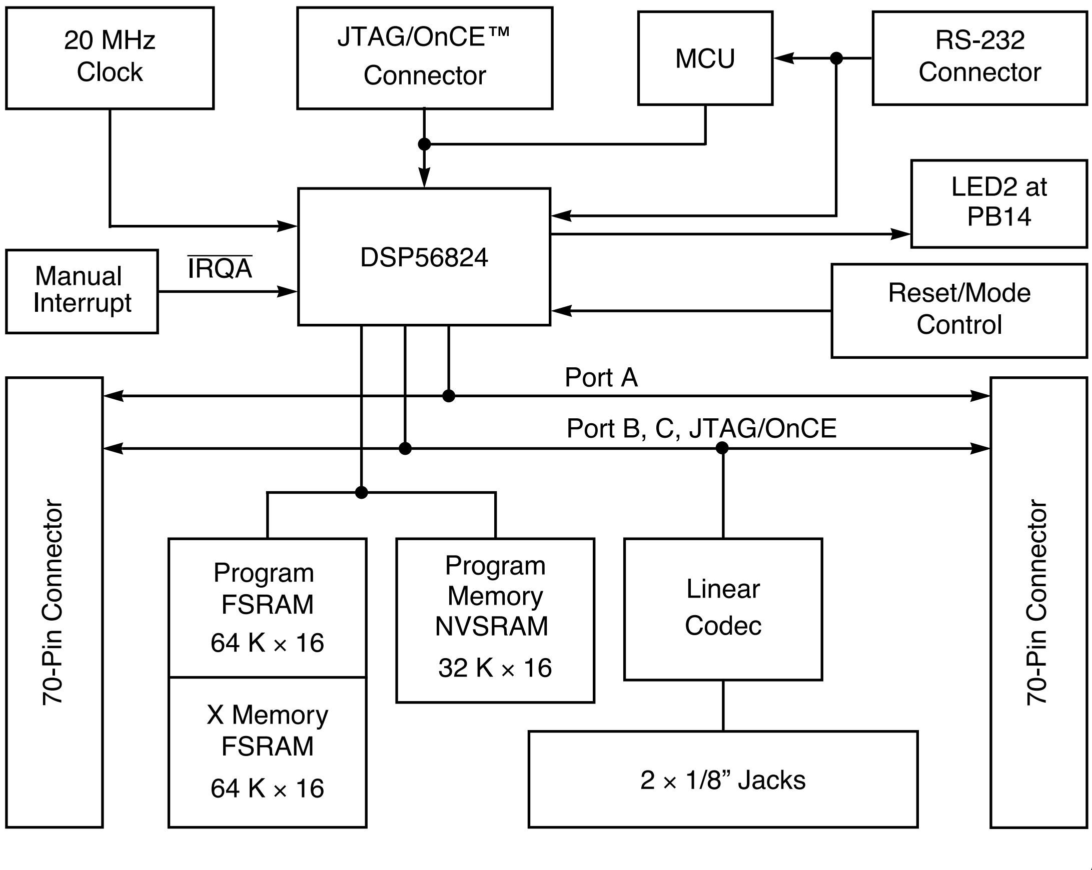


Figure 2-1 DSP56824ADM Functional Block Diagram

2.3.1 Fast Static RAM (FSRAM)

The DSP56824ADM uses two banks of 64K × 16-bit Fast Static RAM (Motorola MCM6323A, labelled U6 and U7) for memory expansion. U6 provides program memory, and U7 provides data memory. U6 is addressed for use in the DSP’s program memory space. The FSRAM U7 is addressed for use in the DSP’s data memory space. The on-board jumpers JG3 and JG13 allow configuration of the FSRAM and NVSRAM in the program memory space. The on-board jumper JG4 allows configuration of the FSRAM in the data memory space. Refer to **Table 2-4** on page 2-9 and **Table 2-5** on page 2-10 for setting these jumpers.

2.3.2 Non-Volatile Static RAM (NVSRAM)

The DSP56824ADM provides two 32K × 8-bit NVSRAM memory devices, installed as U9 and U10, to give a total of 32K × 16-bit NVSRAM memory. External Program RAM must be configured for operation in the lower program memory address space ($0000–$7FFF). The NVSRAM memory automatically decodes to the upper program memory space ($8000–$FFFF) when enabled by JG13.

2.4 VOICE CODEC

The DSP56824ADM analog section uses Motorola's MC145483 13-bit linear codec, installed at U17. Refer to the data sheet included with this kit for more information on the MC145483. The DSP56824ADM has 1/8-inch jacks for codec input and output. Codec output jumper JG11 can select one of two separate output load drives. Refer to **Table 2-9** on page 2-11 for a description of the output load options. The codec interfaces to the DSP via the Synchronous Serial Interface (SSI) provided on Port C of the DSP56824. No glue logic is required. The codec clock and frame synchronization are provided by the SSI. Jumper JG5 allows the user to disconnect the on-board codec completely. See **Table 2-6** on page 2-11. This frees the SSI port on the DSP56824 for other peripheral use.

2.5 OTHER DSP56824ADM FEATURES

The DSP56824ADM provides these additional user features:

- User-replaceable clock oscillator
- Two on-board LED indicators
- Two on-board pushbutton switches
- Four on-board test points

These features are described in the following subsections.

2.5.1 Clock Oscillator

A user-replaceable clock oscillator, U12, is provided to allow custom configuration of the clock for the DSP56824. Any oscillator speed up to the maximum speed of the DSP can be used. JG9 (see **Clock Input Selection** on page 2-7) allows using 3.3 V or 5 V oscillators.

2.5.2 LED Indicators

Two on-board Light-Emitting Diodes (LEDs) are provided. LED1 is a power indicator that shows when power is applied to the DSP56824ADM board. LED2 is a debugging indicator. See **PB14 Indicator LED Configuration** on page 2-12 for more information on LED2. Both LEDs are located next to J7, the power input connector.

2.5.3 Pushbutton Switches

Two on-board pushbutton switches are provided. S1 allows the user to generate a hardware reset to the DSP56824. The $\overline{\text{RESET}}$ line on the DSP56824 is asserted low when S1 is depressed. S2 asserts $\overline{\text{IRQA}}$ when it is depressed. S1 and S2 are located near J4 and J5, the codec input and output connectors.

2.5.4 Test Points

Four on-board test points are provided to allow for voltage reference connections. TP1 and TP2 are connected to analog ground. TP3 is connected to the 3.3 V supply. TP4 is connected to the 5 V supply.

2.6 JUMPER CONFIGURATION

The DSP56824ADM board includes a number of configuration jumpers that allow the user to modify the way in which the board is used in a particular application. The following paragraphs give a detailed description of the function of the jumpers.

2.6.1 Clock Input Selection

The clock input to the DSP is selected by jumper group JG1. There are two options for the clock input selection. The DSP clock source can be the on-board user clock oscillator.

Alternatively, an external clock input can be connected via the J2 expansion connector or applied directly to JG1 Pin 3. See **Table 2-1**.

Table 2-1 Clock Source Selection

Clock Source	JG1
20 MHz user oscillator clock (default)	1–2
External clock CLOCK_IN on J2 pin 1	3–4

Note: The DSP56824ADM is factory configured to use the on-board 20 MHz clock oscillator (U12).

2.6.2 User Clock Oscillator V_{CC} Setting

Jumper group JG9 is used to select the power source (3.3 V or 5.0 V) for the Clock Oscillator (U12). Jumpering pins 1–2 on JG9 selects +3.3 V. Jumpering pins 2–3 on JG9 selects 5.0 V, the default setting. The output signal at the clock oscillator is buffered and inverted before being sent to the DSP. See **Table 2-2** for details.

Table 2-2 Oscillator V_{CC} Selection

JG9	Comment
1–2	Clock V_{CC} is +3.3 V
2–3	Clock V_{CC} is +5.0 V (default)

Note: The DSP56824ADM is factory configured for clock V_{CC} to be +5 V.

2.6.3 Operating Mode Selection

Jumper group JG2 selects the operating mode of the DSP after reset. Refer to the DSP56824 User’s Manual for a complete description of the chip’s operating modes. Programs can be loaded from NVSRAM by configuring the DSP to exit reset in Operating Mode 0 or 2. **Table 2-3** shows the JG2 selection to achieve any of the four operating modes available on the DSP56824.

Table 2-3 Operating Mode Selection

Operating Mode	JG2	Comment
0	1–2, 3–4	Bootstrap from byte-wide EPROM
1	3–4	Bootstrap from SPI0 or SSI Port
2	1–2	Normal Expanded P:$E000 (default)
3	No jumpers	Development P:$0000

Note: The DSP56824ADM is factory configured to exit from reset in Mode 2.

2.6.4 Program Memory Configuration

Jumper group JG3 selects the external program static RAM memory configuration. For fastest operation with the installed 10 ns FSRAM, jumper pins JG3 1–2 and 3–4, and configure the Bus Control Register (BCR) for zero wait states. Program memory will then occupy address range P:$0–$FFFF.

If the NVSRAM is used, jumper pins JG3 5–6 and JG13 1–2. The program Static RAM occupies address range P:$0–$7FFF, and the NVSRAM occupies address range P:$8000–$FFFF. The delay from gating address line A15 with $\overline{\text{PS}}$ requires that the BCR must be configured for at least one wait state while executing out of external program memory. The NVSRAM offers a means of executing programs and loading memory as required from its non-volatile memory after exiting reset. See **Table 2-4** for JG3 and JG13 program memory configuration.

Table 2-4 Program Memory Configuration

Configuration	JG3	JG13	Comment
0 (default)	5–6	1–2	FSRAM: P:$0000–$7FFF, zero wait states NVSRAM: P:$8000–$FFFF
1	1–2, 3–4	NC	FSRAM: P:$0000–$FFFF, zero wait states
2	5–6	NC	FSRAM: P:$0000–$7FFF, one wait state P:$8000–$FFFF User expanded memory
3	1–2	NC	FSRAM: P:$0000–$7FFF, zero wait states P:$8000–$FFFF Shadow of P:$0000–$7FFF
4	NC	1–2	NVSRAM: P:$8000–$FFFF

Note: The DSP56824ADM is factory configured for program memory in the range P:$0000–$7FFF (FSRAM) and P:$8000–$FFFF (NVSRAM).

2.6.5 Data Memory Configuration

Jumper group JG4 is used to select one of two DSP external data memory options. The default setting is JG4 1–2 and 3–4. Data memory is setup from P:0000–$FFFF. See **Table 2-5** for JG4 data memory configuration.

Table 2-5 Data Memory Configuration

Configuration	JG4	Comment
0 (default)	1–2, 3–4	X:0000–$FFFF, zero wait states
1	5–6	X:0000–$7FFF, one wait state X:8000–$FFFF User expanded memory
2	1–2	X:0000–$7FFF, zero wait states X:$8000–$FFFF Shadow of X:0000–$7FFF

Note: The DSP56824ADM is factory configured for data memory in the range X:0000–$FFFF.

2.6.6 Codec Configuration

Jumper groups JG5, JG11, JG16, and JG17 enable and configure the on-board MC145483 codec.

2.6.6.1 Codec Enabling

Jumper group JG5 configures the on-board codec. The default setting is JG5 1–2, 3–4, 5–6, and 7–8 for the MC145483 codec. If a different codec or another peripheral requires the use of PC8/STD, PC9/SRD, PC10/STCK, and PC11/STFS, all the jumpers should be removed from JG5. See **Table 2-6** for JG5 codec configuration.

Table 2-6 Codec Selection

Configuration	JG5	Comment
On-board codec (default)	1–2, 3–4, 5–6, 7–8	Enable MC145483 codec
User application	no jumpers	Other peripheral

Note: The DSP56824ADM is factory configured for the MC145483 codec.

2.6.6.2 Codec Input Connector Signal Selection

Jumper group JG16 is used to select which signal on J4 is sent to the codec. See **Table 2-7** for JG16 configuration information.

Table 2-7 Codec Input Signal Selection

JG16	Comment
NC (default)	Input signal from tip of jack
1–2	Input signal from tip and ring of jack

2.6.6.3 Codec Output Connector Signal Selection

Jumper group JG17 is used to select which pins on J5 provide the output signal from the codec. See **Table 2-8** for JG17 configuration information.

Table 2-8 Codec Output Signal Selection

JG17	Comment
NC	Output signal goes to tip of jack
1–2 (default)	Output signal goes to tip and ring of jack

2.6.6.4 Codec Output Load Selection

Jumper group JG11 is used to select the output drive capability of the codec with respect to analog ground. See **Table 2-9** for JG11 configuration information.

Table 2-9 Codec Output Selection

JG11	Comment
1–2 (default)	1.7 V peak @ 300 Ω load
2–3	0.8 V peak @ 2kΩ load

Note: The DSP56824ADM is factory configured for codec output of 1.7 V into a 300 Ω load.

2.6.7 RS-232 Serial Communication Configuration

The DSP56824ADM includes a DB9 connector for an RS-232 serial link. Jumpering JG7 pins 3–5 and 4–6 connects the RS-232 serial port to the DSP. Although there is no hardware support for RS-232 on the DSP56824, software on the DSP may use the serial port by program control of pins PB0 and PB1.

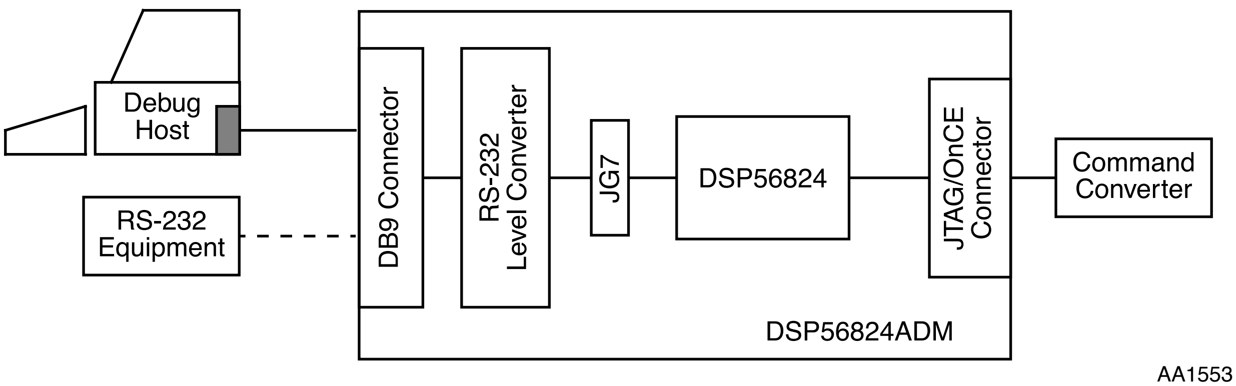


Figure 2-2 RS-232 Serial Communication Options

Table 2-10 Serial Communication Configuration

Configuration	JG7	Comment
DSP GPIO pins (default)	3–5, 4–6	Available for use by DSP software
MCU serial port	1–3, 2–4	Serial debug port for DSP56824ADM system

Note: The DSP56824ADM is factory configured with the serial port connected to the DSP.

2.6.8 PB14 Indicator LED Configuration

LED2 is provided as a simple tool for assisting with software debugging via the PB14 signal. Jumper group JG12 is used to set up LED2 as a status indicator. If JG12 is not

jumpered, PB14 functions as a GPIO pin with a 10 kΩ pull-up resistor. Jumpering JG12 1–2 connects PB14 to ground through LED2 and a 150 Ω current-limiting resistor. LED2 illuminates when the user software sets pin PB14 high. See **Table 2-11**.

Table 2-11 PB14 LED Drive Selection

Configuration	JG12	Comment
PB14 as indicator (default)	1–2	PB14 drives LED2
PB14 pull-up	NC	PB14 is GPIO pin

Note: The DSP56824ADM is factory configured with PB14 operating as an output to drive LED2.

2.6.9 Power Input Selection

Jumper group JG14 is used to select the input voltage source to the DSP56824ADM board. See **Table 2-12** for JG14 configuration information.

Table 2-12 Power Input Selection

Configuration	JG14	Comment
0 (default)	3–4, 5–6, 7–8	9–12 VDC from power jack J7 to on-board voltage regulators
1	1–3, 6–8	User voltage from power jack J7 directly to V_{CC} and V_{DD} power planes (on-board voltage regulators are bypassed)

2.6.10 Reset Control Selection

Jumper group JG15 is used to select the source of the DSP56824's $\overline{\text{RESET}}$ signal. See **Table 2-13** for JG15 configuration information.

Table 2-13 $\overline{\text{RESET}}$ Selection

Configuration	JG15	Comment
0 (default)	1–2	On-board 3.3 V reset logic
1	NC	Reset from external source: • Expansion connector J2 • JTAG/OnCE connector J3

2.6.11 PB15 Pull Up/Pull Down Selection

Jumper group JG10 is used to pull up or down the dual-function signal pin PB15 for DSP reading at reset. This is required to compensate for nonlinear frequency response in the clock circuit. For clock frequencies in the range of 32 kHz–2 MHz, JG10 1–2 should be jumpered to pull down PB15. For clock frequencies in the range of 2 MHz–70 MHz, remove the jumper to pull up PB15. See **Table 2-14** for PB15 configuration information.

Table 2-14 PB15 Selection

Configuration	JG10	Comment
PB15 pull-up (default)	Open	Clock frequencies 2 MHz to maximum DSP frequency
PB15 pull-down	1–2	Clock frequencies 32 kHz–2 MHz

Note: The DSP56824ADM is factory configured for clock frequencies between 2 MHz and the maximum frequency of the DSP.

2.7 DSP56824ADM CONNECTOR DESCRIPTIONS

There are seven connectors on the DSP56824ADM. **Table 2-15** describes the connectors.

Table 2-15 DSP56824ADM Connectors

Connector	Comment
J1	70-pin Expansion Connector 1 (bottom of board)
J2	70-pin Expansion Connector 2 (bottom of board)
J3	14-pin JTAG/OnCE Module Interface to DSP
J4	1/8″ Mono Line Input Jack to Codec
J5	1/8″ Stereo Line Output Jack from Codec
J6	DB9 RS-232 serial Interface connector
J7	Power Connector

2.7.1 Expansion Connector 1

Expansion Connectors J1 and J2 are used to make connections to the DSP pins. **Table 2-16** lists the DSP pins that are accessed on Expansion Connector J1.

Table 2-16 DSP56824ADM J1 Bus Connector Description

J1			
Pin #	**Signal**	**Pin #**	**Signal**
1	V_{CC}	2	V_{CC}
3	V_{CC}	4	A15
5	$\overline{WR}$	6	A14
7	$\overline{RD}$	8	A13
9	$\overline{PS}$	10	A12
11	$\overline{DS}$	12	A11
13	V_{CC}	14	A10
15	V_{CC}	16	A9
17	V_{CC}	18	A8

Table 2-16 DSP56824ADM J1 Bus Connector Description (Continued)

J1			
Pin #	**Signal**	**Pin #**	**Signal**
19	V_{CC}	20	A7
21	V_{CC}	22	A6
23	NC	24	A5
25	GND	26	A4
27	GND	28	A3
29	GND	30	A2
31	GND	32	A1
33	GND	34	A0
35	GND	36	GND
37	GND	38	D0
39	GND	40	D1
41	GND	42	D2
43	GND	44	D3
45	GND	46	D4
47	GND	48	D5
49	GND	50	D6
51	GND	52	D7
53	GND	54	D8
55	GND	56	D9
57	GND	58	D10
59	NC	60	D11
61	NC	62	D12
63	NC	64	D13
65	ROM_DIS	66	D14
67	GND	68	D15
69	GND	70	GND

2.7.2 Expansion Connector 2

Table 2-17 lists the DSP pins that are accessed on Expansion Connector J2.

Table 2-17 DSP56824ADM J2 Bus Connector Description

J2			
Pin #	**Signal**	**Pin #**	**Signal**
1	CLOCK_IN	2	$\overline{\text{RESET}}$
3	PC15/TIO2	4	+5V
5	PC14/TIO1	6	+5V
7	PC13/SRFS	8	NC
9	PC12/SRCK	10	+12V
11	PC11/STFS	12	+12V
13	PC10/STCK	14	NC
15	PC9/SRD	16	V_{CC}
17	PC8/STD	18	V_{CC}
19	PC7/$\overline{\text{SS1}}$	20	V_{CC}
21	PC6/SCK1	22	V_{CC}
23	PC5/MOSI1	24	V_{CC}
25	PC4/MISO1	26	V_{CC}
27	PC3/$\overline{\text{SS0}}$	28	MODA/$\overline{\text{IRQA}}$
29	PC2/SCK0	30	MODB/$\overline{\text{IRQB}}$
31	PC1/MOSI0	32	NC
33	PC0/MISO0	34	NC
35	CLKO	36	GND
37	PB15	38	GND
39	PB14	40	GND

Table 2-17 DSP56824ADM J2 Bus Connector Description (Continued)

J2			
Pin #	**Signal**	**Pin #**	**Signal**
41	PB13	42	GND
43	PB12	44	GND
45	PB11	46	GND
47	PB10	48	MODA
49	PB9	50	MODB
51	PB8	52	$\overline{\text{RESET_IN}}$
53	PB7	54	$\overline{\text{IRQA_IN}}$
55	PB6	56	$\overline{\text{IRQB_IN}}$
57	PB5	58	TDO
59	PB4	60	TMS
61	PB3	62	TCK
63	PB2	64	TRST/$\overline{\text{DE}}$
65	PB1	66	TDI
67	PB0	68	GND
69	GND	70	GND

2.7.3 JTAG/OnCE Connector

Connector J3 is used to connect the DSP56824ADM to a host development system using a Command Converter and Host Computer Interface Card. The ADS software controls the chip execution by accessing the OnCE module controller via the JTAG port interface and provides facilities for software development and debugging.

This connector may allow the user to access the JTAG Test Access Port (TAP) directly. The pin out of this connector is shown in **Table 2-18**.

Table 2-18 DSP56824ADM J3 JTAG/OnCE Description

J3			
Pin #	**Signal**	**Pin #**	**Signal**
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	NC	8	KEY
9	$\overline{\text{J_RESET}}$	10	TMS
11	V_{CC}	12	NC
13	TRST/$\overline{\text{DE}}$	14	TRST/$\overline{\text{DE}}$

2.7.4 Codec Jacks

J4 and J5 are stereo jacks that allow the user to send and receive analog signals to and from the on-board codec. J4 enables the user to apply an input signal to the on-board codec. The pinout of this connector is listed in **Table 2-19**.

Table 2-19 DSP56824ADM J4 Line In Description

Connector	Signal
Barrel	ANALOG GND
Tip	LINE IN
Ring	LINE IN (optional)

J5 enables the user to send an output signal from the on board codec. The pinout of this connector is listed in **Table 2-20**.

Table 2-20 DSP56824ADM J5 Line Out Description

Connector	Signal
Barrel	ANALOG GND
Tip	LINE OUT
Ring	LINE OUT (optional)

Note: J4 and J5 are stereo jacks. However, only mono audio capability is provided on the DSP56824ADM.

2.7.5 RS-232 Serial Communication Interface Connector

The RS-232 port J6 can be used as a communications port by the DSP. See **Section 2.6.7 RS-232 Serial Communication Configuration** on page 2-12. **Table 2-21** describes the signals available on J6, the serial connector.

Table 2-21 DSP56824ADM Serial Connector Description

J6			
Pin #	**Signal**	**Pin #**	**Signal**
1	OC0 (+5 V)	2	RX
3	TX	4	DTR (+5 V)
5	GND	6	DSR (+5 V)
7	RTS (n/c)	8	CTS
9	RI (n/c)		

Note: OC0, DTR, and DSR are Wire OR-ed together and are used to drive the microcontroller's $\overline{\text{RESET}}$ signal.

2.7.6 Power Source Connector

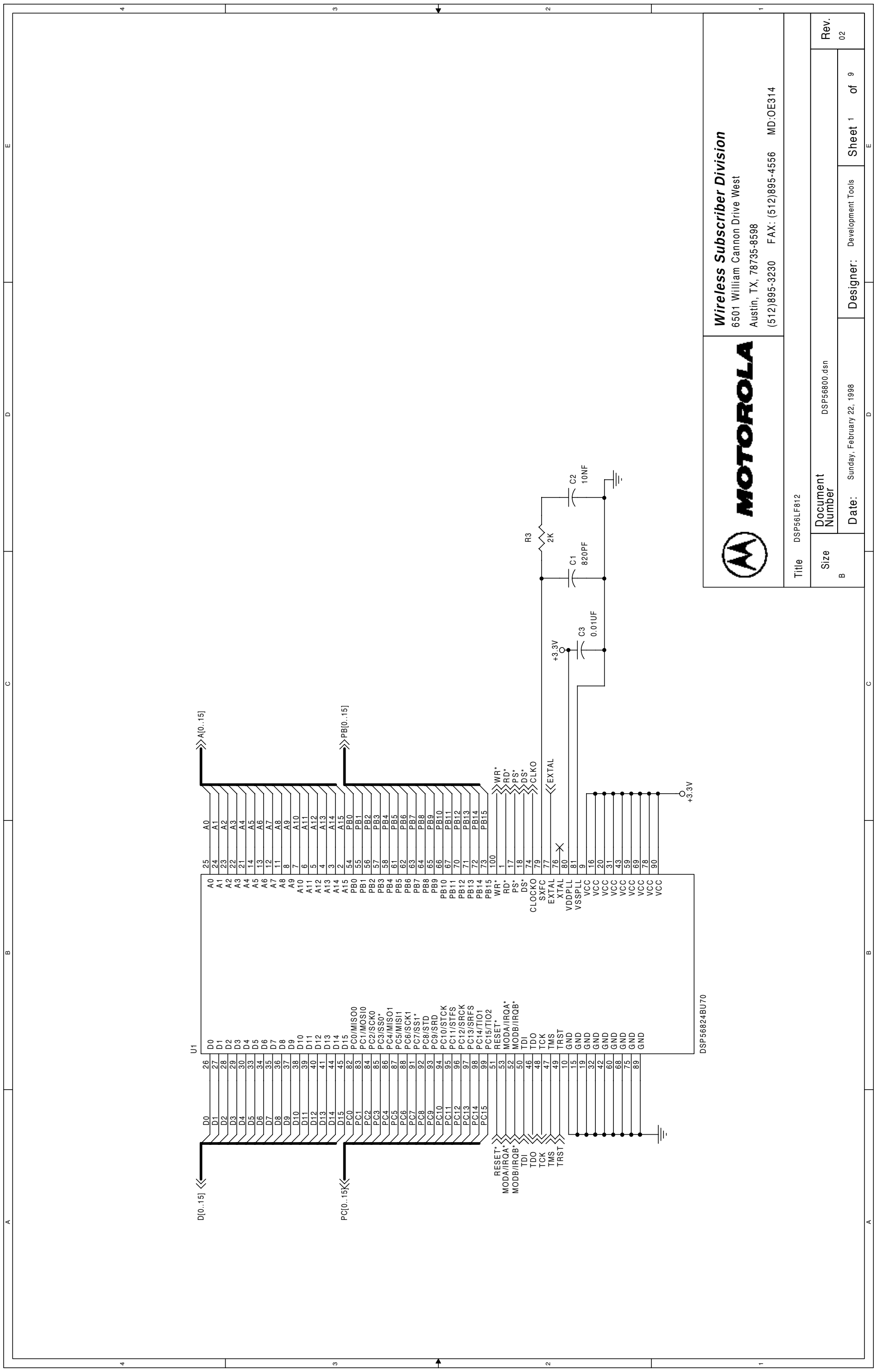
Input voltage range is 9–12 V dc at 500 mA. **Table 2-22** shows this connector pins description.

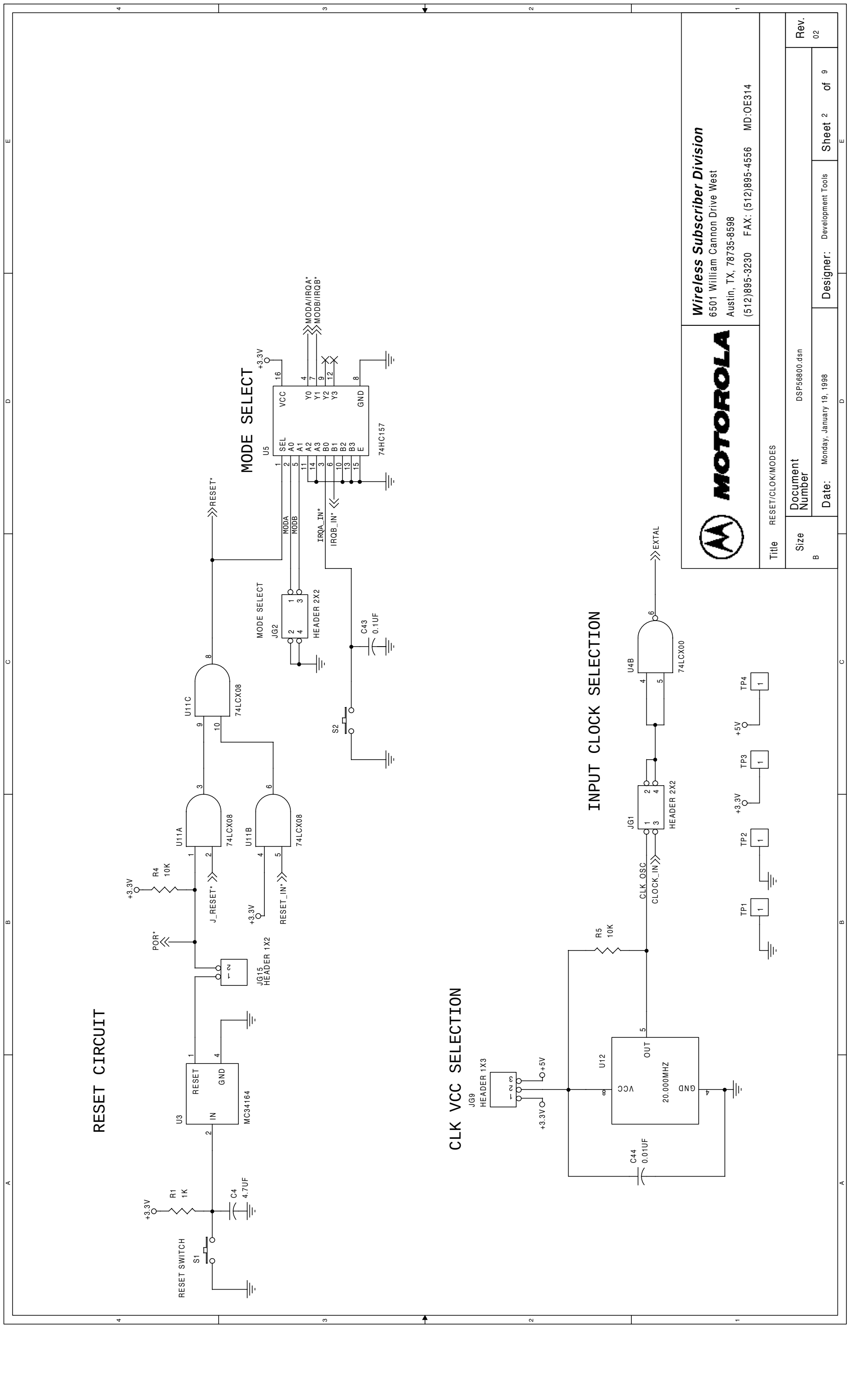
Table 2-22 DSP56824ADM J7 Power Source Connector Description

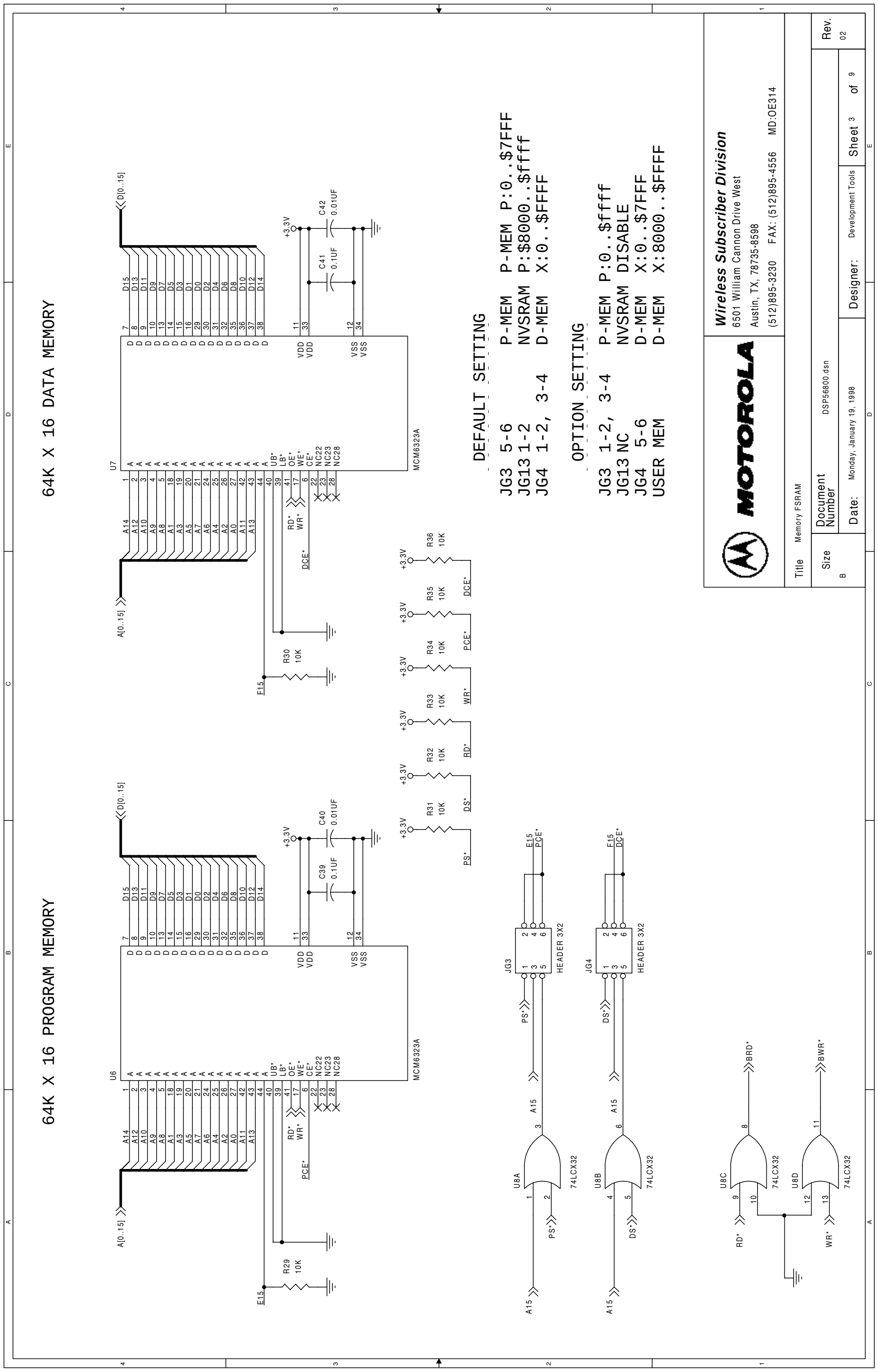
Connector	Signal
Inner connector	V_{CC} IN
Outer ring	GND

APPENDIX A

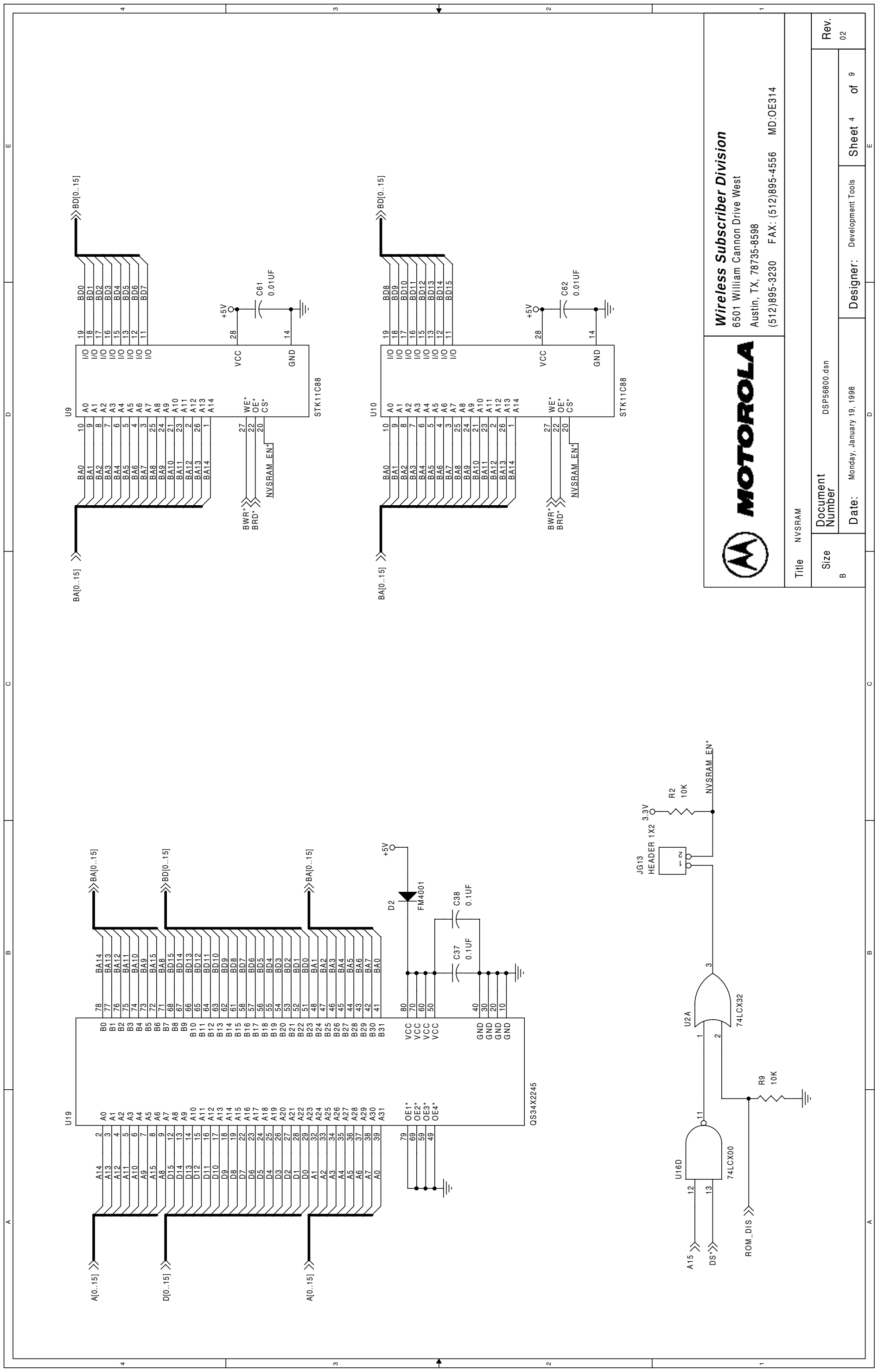
DSP56824ADM SCHEMATICS

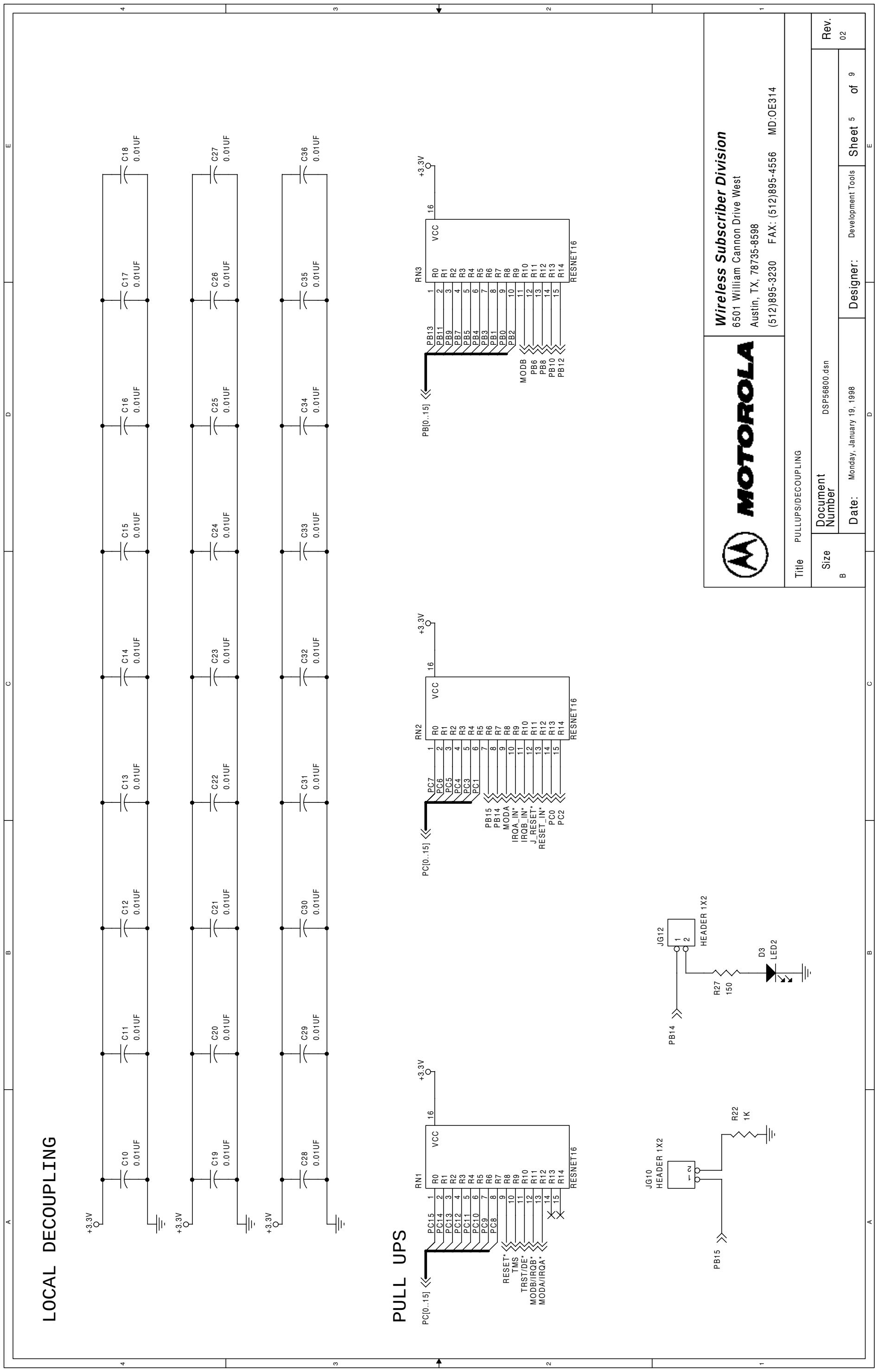

Wireless Subscriber Division
6501 William Cannon Drive West
Austin, TX, 78735-8598
(512)895-3230 FAX: (512)895-4556 MD:OE314
Title DSP56LF812
Size B
Document Number DSP56800.dsn
Rev. 02
Date: Sunday, February 22, 1998
Designer: Development Tools
Sheet 1 of 9

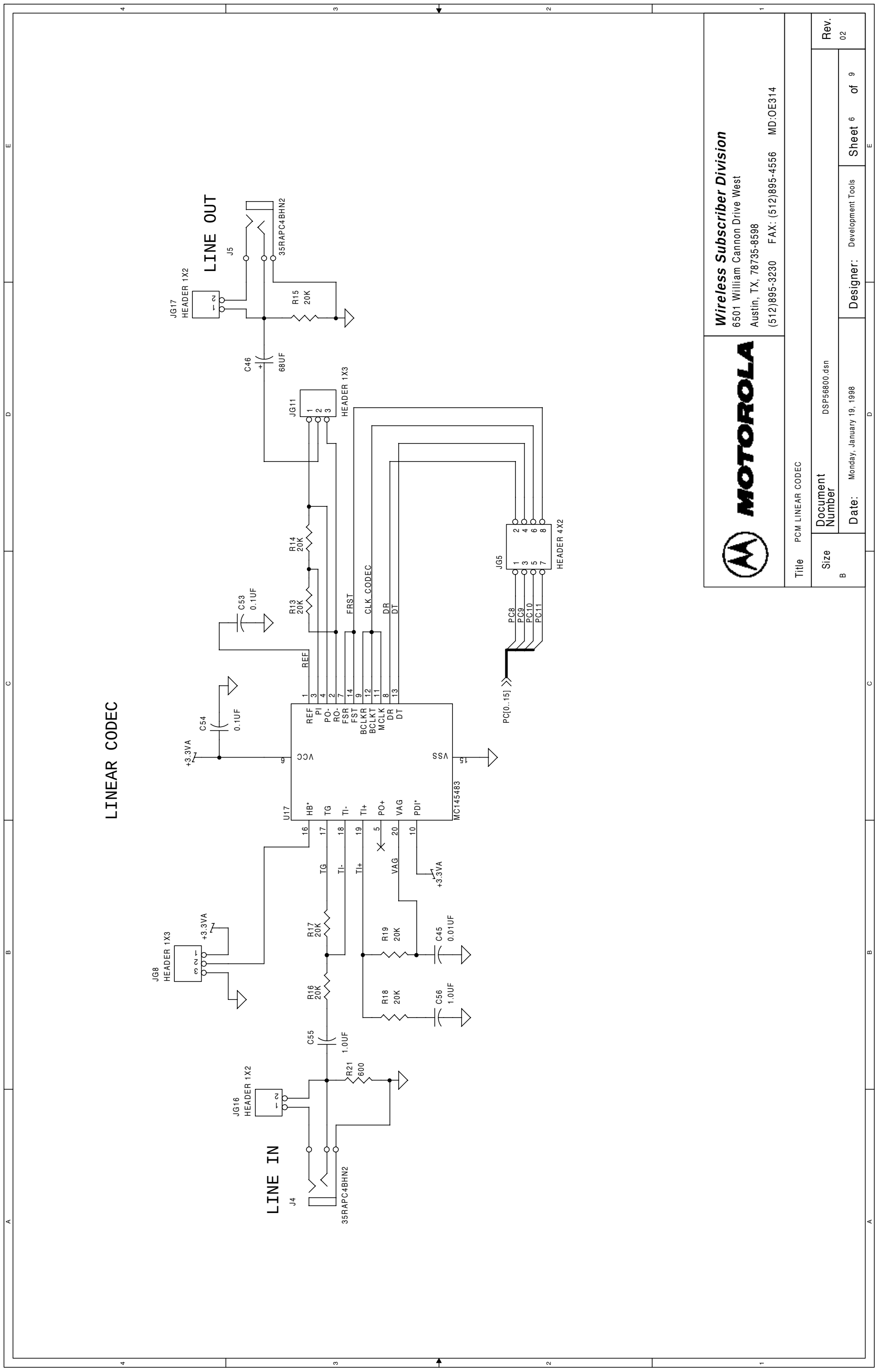

RESET CIRCUIT
MODE SELECT
CLK VCC SELECTION
INPUT CLOCK SELECTION
Wireless Subscriber Division
6501 William Cannon Drive West
Austin, TX, 78735-8598
(512)895-3230 FAX: (512)895-4556 MD:OE314
Title RESET/CLK/MODES
Size B
Document Number DSP56800.dsn
Date: Monday, January 19, 1998
Designer: Development Tools
Sheet 2 of 9
Rev. 02

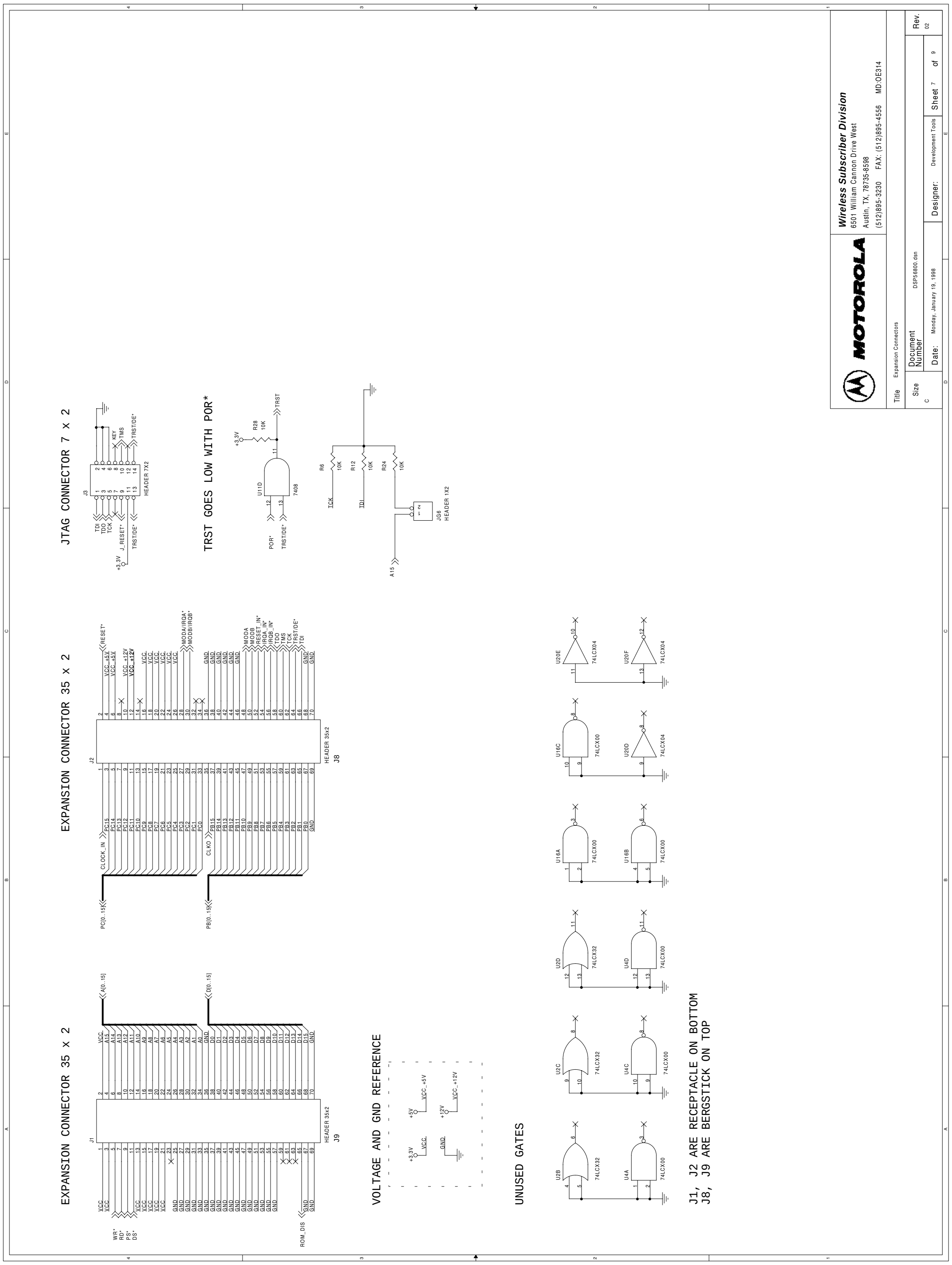


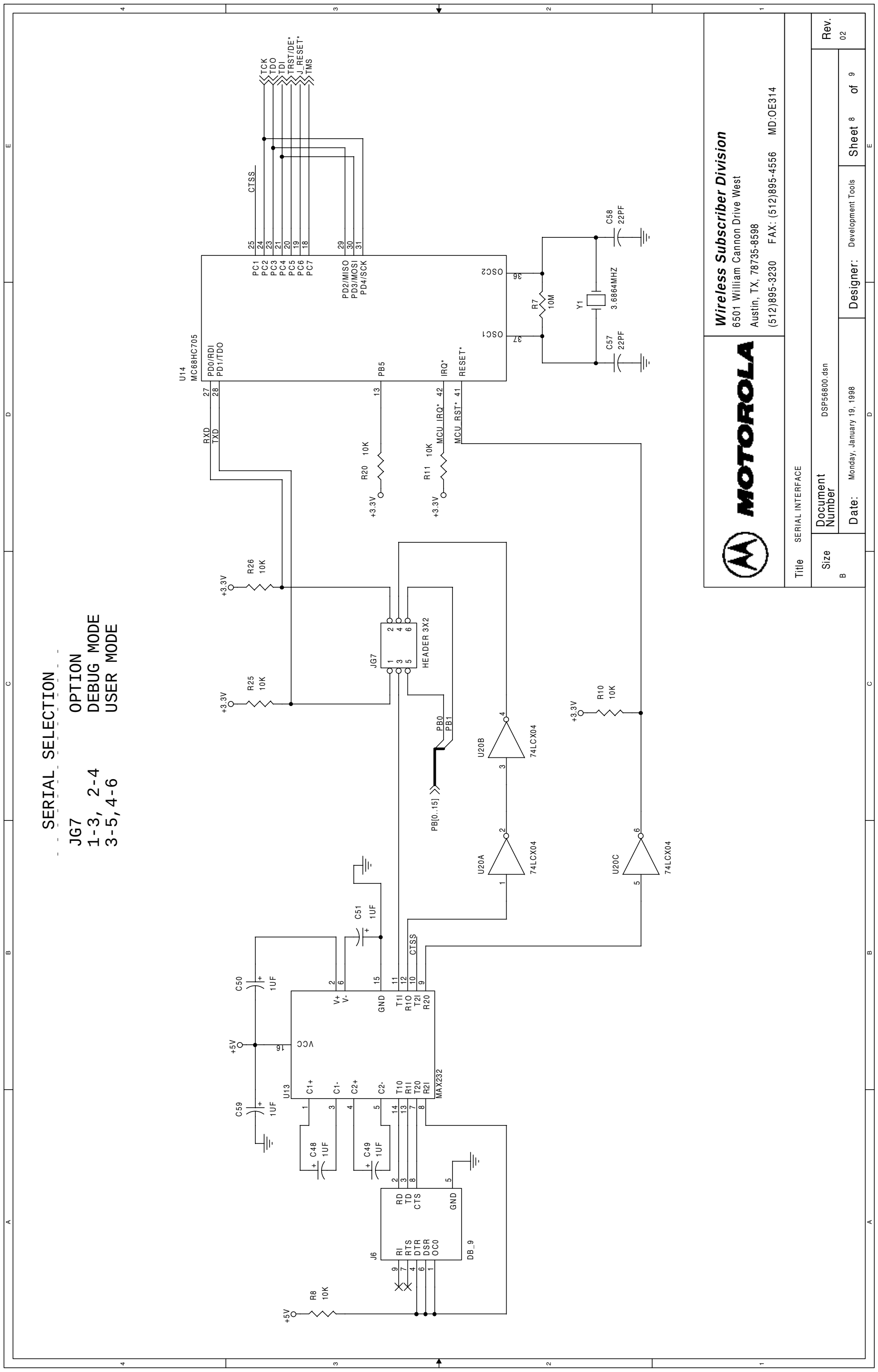
64K X 16 PROGRAM MEMORY
64K X 16 DATA MEMORY
MCM6323A
74LCX32
HEADER 3X2
DEFAULT SETTING
JG3 5-6 P-MEM P:0..$7FFF
JG13 1-2 NVSRAM P:$8000..$ffff
JG4 1-2, 3-4 D-MEM X:0..$FFFF
OPTION SETTING
JG3 1-2, 3-4 P-MEM P:0..$ffff
JG13 NC NVSRAM DISABLE
JG4 5-6 D-MEM X:0..$7FFF
USER MEM D-MEM X:8000..$FFFF
MOTOROLA
Wireless Subscriber Division
6501 William Cannon Drive West
Austin, TX, 78735-8598
(512)895-3230 FAX: (512)895-4556 MD:OE314
Title Memory FSRAM
Size B
Document Number DSP56800.dsn
Rev. 02
Date: Monday, January 19, 1998
Sheet 3 of 9
Designer: Development Tools

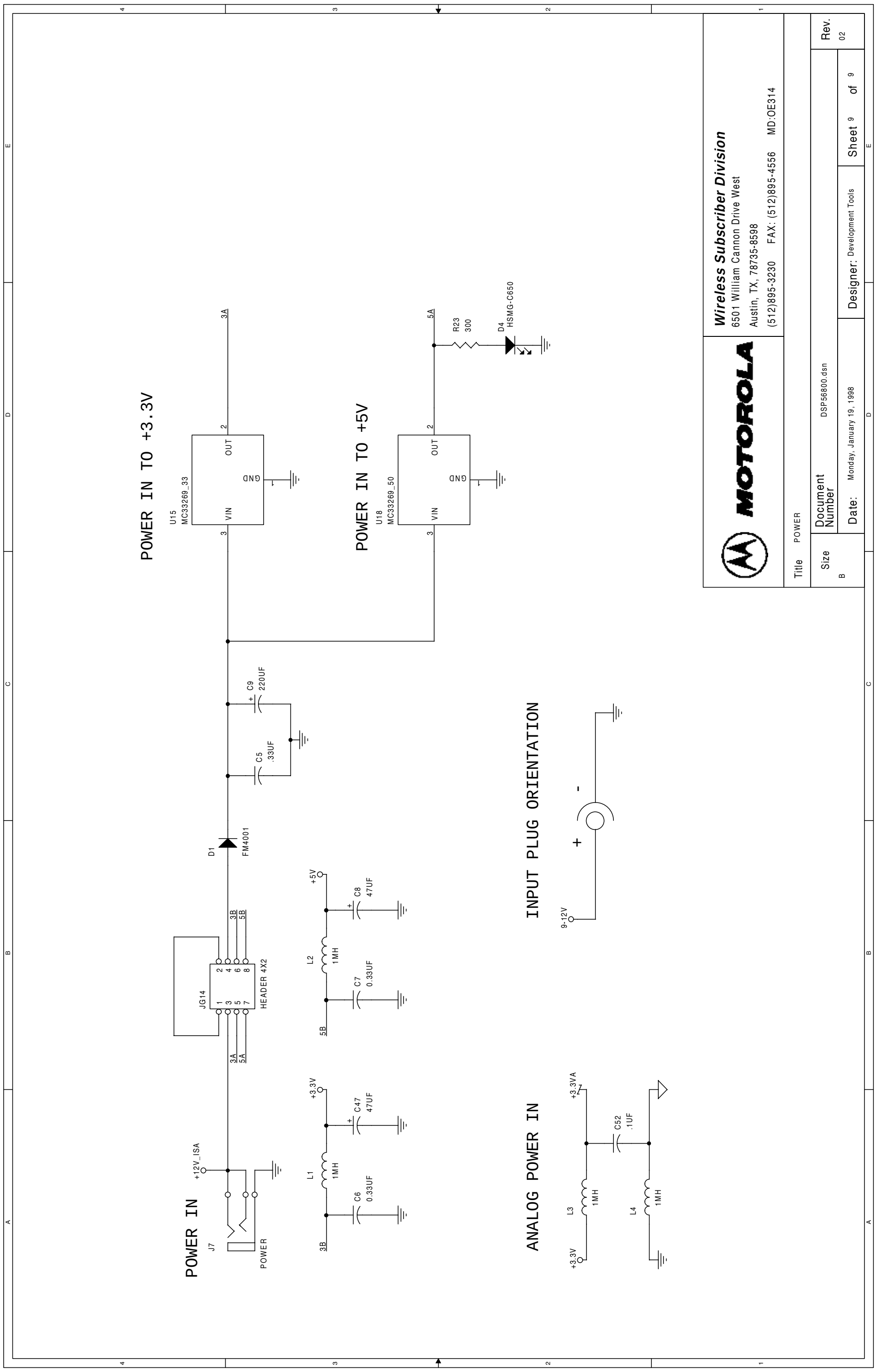

Wireless Subscriber Division
6501 William Cannon Drive West
Austin, TX, 78735-8598
(512)895-3230 FAX: (512)895-4556 MD:OE314
Title NVSRAM
Size B
Document Number DSP56800.dsn
Rev. 02
Date: Monday, January 19, 1998
Designer: Development Tools
Sheet 4 of 9
U19 QS34X2245
U9 STK11C88
U10 STK11C88
U2A 74LCX32
U16D 74LCX00
JG13 HEADER 1X2
NVSRAM_EN*
ROM_DIS


LOCAL DECOUPLING
PULL UPS
Wireless Subscriber Division
6501 William Cannon Drive West
Austin, TX, 78735-8598
(512)895-3230 FAX: (512)895-4556 MD:OE314
MOTOROLA
Title PULLUPS/DECOUPLING
Size B
Document Number DSP56800.dsn
Rev. 02
Date: Monday, January 19, 1998
Designer: Development Tools
Sheet 5 of 9


LINEAR CODEC
LINE IN
LINE OUT
MC145483
PCM LINEAR CODEC
Wireless Subscriber Division
6501 William Cannon Drive West
Austin, TX, 78735-8598
(512)895-3230 FAX: (512)895-4556 MD:OE314
DSP56800.dsn
Monday, January 19, 1998
Development Tools
Sheet 6 of 9
Rev. 02


EXPANSION CONNECTOR 35 x 2
EXPANSION CONNECTOR 35 x 2
JTAG CONNECTOR 7 x 2
TRST GOES LOW WITH POR*
VOLTAGE AND GND REFERENCE
UNUSED GATES
J1, J2 ARE RECEPTACLE ON BOTTOM
J8, J9 ARE BERGSTICK ON TOP
MOTOROLA
Wireless Subscriber Division
Title
Document Number
Date:
Designer:
Sheet
Rev.


SERIAL SELECTION
JG7 OPTION
1-3, 2-4 DEBUG MODE
3-5,4-6 USER MODE
MOTOROLA
Wireless Subscriber Division
6501 William Cannon Drive West
Austin, TX, 78735-8598
(512)895-3230 FAX: (512)895-4556 MD:OE314
Title SERIAL INTERFACE
Size B
Document Number DSP56800.dsn
Rev. 02
Date: Monday, January 19, 1998
Designer: Development Tools
Sheet 8 of 9


POWER IN TO +3.3V
U15
MC33269_33
VIN
OUT
GND
POWER IN TO +5V
U18
MC33269_50
R23
300
D4
HSMG-C650
C9
220UF
C5
.33UF
D1
FM4001
JG14
HEADER 4X2
POWER IN
+12V_ISA
J7
POWER
L1
1MH
L2
C6
0.33UF
C7
0.33UF
C8
47UF
C47
47UF
+3.3V
+5V
INPUT PLUG ORIENTATION
9-12V
ANALOG POWER IN
+3.3VA
L3
L4
C52
.1UF
Wireless Subscriber Division
6501 William Cannon Drive West
Austin, TX. 78735-8598
(512)895-3230 FAX: (512)895-4556 MD:OE314
Title POWER
Size B
Document Number DSP56800.dsn
Rev. 02
Date: Monday, January 19, 1998
Designer: Development Tools
Sheet 9 of 9

APPENDIX B

DSP56824ADM BILL OF MATERIALS

B.1 ELECTRICAL PARTS LIST

Qty	Description	Ref. Designators	Vendor Part #
Integrated Circuits			
1	DSP56824BU70	U1	Motorola
2	MC74LCX32DT	U2, U8	Motorola
1	MC34164D-3	U3	Motorola
2	MC74LCX00DT	U4, U16	Motorola
1	MC74HC157DT	U5	Motorola
2	MCM6323ATS10	U6, U7	Motorola
1	STK11C88-N25	U9, U10	Simtek
1	MC74LCX08DT	U11	Motorola
1	SG 531P—20MHZ	U12	SG
1	MAX232CSE	U13	Maxim
1	MC68HC705C4ACFB	U14	Motorola
1	MC33269DT-3.3	U15	Linear Technologies
1	MC145483DW	U17	Motorola
1	MC33269DT-5.0	U18	Motorola
1	QS34X2245Q3	U19	Quality Semiconductor
1	MC74LCX04DT	U20	Motorola
Crystal			
1	3.6864 MHz	Y1	ECS ECS-36-20-7

Qty	Description	Ref. Designators	Vendor Part #
Resistors			
1	150 Ω	R27	Venkel CR0805-10W-1500FT
1	300 Ω	R23	Venkel CR0805-10W-3000FT
1	600 Ω	R21	Venkel CR0805-10W-6010FT
2	1 kΩ	R1, R22	Venkel CR0805-10W-1001FT
1	2 kΩ	R3	Venkel CR0805-10W-2001FT
16	10 kΩ	R2, R4–R6, R8–R12, R20, R24–R26, R28–R36	Venkel CR0805-10W-1002FT
7	20 kΩ	R13–R19	Venkel CR0805-10W-2002FT
1	10 MΩ	R7	Venkel CR0805-10W-1005FT
Resistor Networks			
3	10 kΩ	RN1–RN3	Bourns 2NSB16-TJ2-103
Inductors			
4	1 mH	L1–L4	Murata BL01RN1-A62
LEDs			
2	LED	LED1, LED2	Hewlett-Packard HSMG-C650
Diode			
2	FM4001	D1, D2	Central Semiconductor CMR1-02M

Qty	Description	Ref. Designators	Vendor Part #
Capacitors			
1	820 pF	C1	Venkel C0805COG500-821JNE
1	0.01 μF	C2	Venkel C0805X7R500-103KNE
4	0.1 μF	C52–C54, C60	Venkel C1206X7R250-104KNE
37	0.01 μF	C3, C10–C45, C62	Venkel C1206X7R500-103KNE
2	1 μF	C55, C56	Venkel C1206X7R250-105KNE
1	220 μF	C9	Panasonic ECEV1CA221P
2	47 μF	C8, C47	Venkel TA006TCM476KDR
1	68 μF	C46	Venkel TA006TCM686KDR
3	0.33 μF	C5, C6, C7	Venkel C1206X7R160-334KNE
5	1.0 μF	C48–C51, C59	Venkel TA016TCM105KAR
1	4.7 μF	C4	Venkel TA006TCM475KAR
2	22 pF	C57, C58	Venkel C1206COG500-220JNE

B.2 HARDWARE PARTS

Qty	Description	Ref. Designator	Vendor Part #
Jumpers			
3	2 × 3 Bergstick	JG3, JG4, JG7	Samtec TSW-1-3-07-S-D
2	2 × 2 Bergstick	JG1, JG2	Samtec TSW-1-2-07-S-D
5	1 × 2 Bergstick	JG6, JG10, JG12, JG13, JG15	Samtec TSW-1-2-07-S-S
2	1 × 3 Bergstick	JG8, JG9	Samtec TSW-1-3-07-S-S
3	2 × 4 Bergstick	JG5, JG11, JG14	Samtec TSW-1-4-07-S-D
Test Points			
4	1 × 1 Bergstick	TP1–TP4	Samtec TSW-1-1-07-S-S
Sockets			
1	100-pin TQFP socket	U10	Yamaichi IC149-100-025-S5
1	4-pin socket	U12	R.N. ICA-043-CE5-30054
Connectors			
2	Audio Connector	J4, J5	Switch Craft 35RAPC4BHN2
1	DB9 Connector	J6	Mouser 152-3409
2	2 × 35 Connector	J1, J2	Samtec FLE-135-01-G-DV
1	2 × 7 Connector	J3	Samtec TSW-1-7-08-S-D-RA
1	Power Connector	J7	Switch Craft RAPC-712
2	2 × 35 Connector	J8, J9	Samtec FW-35-05-L-D-410-175
Switches			
2	SPDT Momentary	S1, S2	Panasonic EVQ-QS205K
Miscellaneous			
21	Shunt	SH1–SH21	Samtec SNT-100-BL-T
4	Rubber Feet	RF1–RF4	Amaton 5186